

EXHIBIT A

Exhibit Designated

**HIGHLY
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Under Stipulated
Protective Order

EXHIBIT B

Exhibit Designated

**HIGHLY
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ATTORNEYS'
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Under Stipulated
Protective Order

EXHIBIT C

**DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION****ATTORNEY DOCKET NO. 10060220-1**

I, a below named inventor, I hereby declare that:

My residence/correspondence post office address and citizenship are as stated below next to my name:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF
DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY**

the specification of which is attached hereto unless the following box is checked:

☒ was filed on April 24, 2006 as US Application Serial No. or PCT International Application
Number 11/410699 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understood the contents of the above-identified specification, including the claims, as amended by any amendment(s) referred to above. I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56.

Foreign Application(s) and/or Claim of Foreign Priority

I hereby claim foreign priority benefits under Title 35, United States Code Section 119 of any foreign application(s) for patent or inventor(s) certificate listed below and have also identified below any foreign application for patent or inventor(s) certificate having a filing date before that of the application on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE FILED	PRIORITY CLAIMED UNDER 35 U.S.C. 119
N/A			YES: <input type="checkbox"/> NO: <input type="checkbox"/>
			YES: <input type="checkbox"/> NO: <input type="checkbox"/>

Provisional Application

I hereby claim the benefit under Title 35, United States Code Section 119(e) of any United States provisional application(s) listed below:

APPLICATION SERIAL NUMBER	FILING DATE
N/A	

U. S. Priority Claim

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (patented/pending/abandoned)
N/A		

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: PRACTITIONERS ASSOCIATED WITH CUSTOMER NUMBER 022878.

Send Correspondence to :

Direct Telephone Calls To:

Customer Number **022878**
AGILENT TECHNOLOGIES, INC.
 Legal Department, DL 429
 Intellectual Property Administration
 P.O. Box 7599
 Loveland, Colorado 80537-0599

Cynthia S. Mitchell
 (970) 679-3136

 OR **Gregory W. Osterloth**
 (303) 291-3204

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Inventor: **Roni Mayder**Citizenship: **U.S.A.**Residence: **San Jose, California**Correspondence Post Office Address: **P.O. Box 7599, Loveland, Colorado 80537-0599**

Inventor's Signature

Date

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**DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION (Continued)**

ATTORNEY DOCKET NO. 10060220-1

Full Name of # 2 Joint Inventor: Pam Stelmacher
Residence: Cupertino, California
Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Citizenship: U.S.A.

Pam Stelmacher
Inventor's Signature

May 9, 2006
Date

Full Name of # 3 Joint Inventor: Edmundo Dela Puente
Residence: Cupertino, California
Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Citizenship: U.S.A.

Edmundo Dela Puente
Inventor's Signature

May 9, 2006
Date

Full Name of # 4 Joint Inventor: John Andberg
Residence: Santa Cruz, California
Correspondence Post Office Address: P.O. Box 7599, Loveland, Colorado 80537-0599

Citizenship: U.S.A.

John Andberg
Inventor's Signature

May 9, 06
Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

Full Name of # Joint Inventor:
Residence:
Correspondence Post Office Address:

Citizenship:

Inventor's Signature

Date

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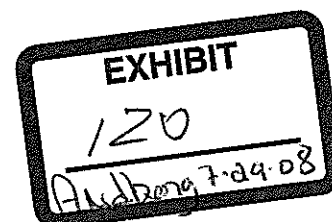
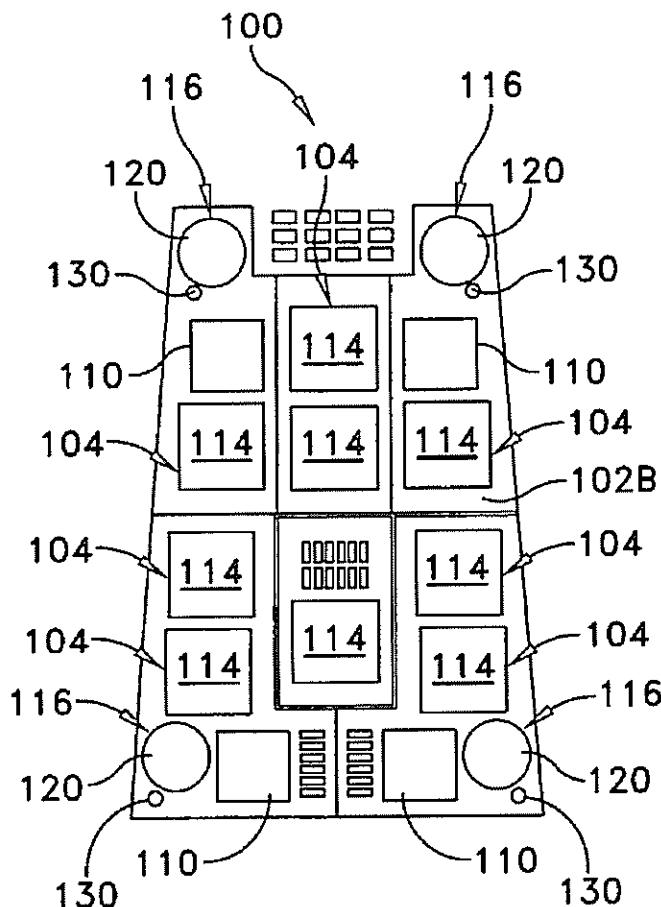
EXHIBIT D



US 20070247140A1

(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2007/0247140 A1**
(43) **Pub. Date: Oct. 25, 2007**(54) **APPARATUS, SYSTEMS AND METHODS FOR PROCESSING SIGNALS BETWEEN A TESTER AND A PLURALITY OF DEVICES UNDER TEST AT HIGH TEMPERATURES AND WITH SINGLE TOUCHDOWN OF A PROBE ARRAY****Publication Classification**(51) **Int. Cl.**
G01R 31/28 (2006.01)
(52) **U.S. Cl.** 324/158.1(57) **ABSTRACT**

Apparatus is for processing signals between a tester and devices under test. In one embodiment, the apparatus includes at least one multichip module. Each multichip module has a plurality of micro-electromechanical switches between a set of connectors to the tester and a set of connectors to devices under test. At least one driver is provided to operate each of the micro-electromechanical switches. A method of processing signals between a tester and devices under test is disclosed. In an embodiment, the method includes connecting the tester and the devices under test with at least one multichip module. Each of the at least one multichip module has a plurality of micro-electromechanical switches between a set of connectors to the tester and a set of connectors to the devices under test. The method includes operating each of the micro-electromechanical switches. Other embodiments are also disclosed.

(76) **Inventors:** Romi Mayder, San Jose, CA (US);
Pam Stellmacher, Cupertino, CA (US);
Edmundo Dela Puente, Cupertino, CA (US); John Andberg, Santa Cruz, CA (US)**Correspondence Address:**
VERIGY
4700 INNOVATION WAY, BLDG D1
FORT COLLINS, CO 80528 (US)
(21) **Appl. No.:** 11/410,699(22) **Filed:** Apr. 24, 2006

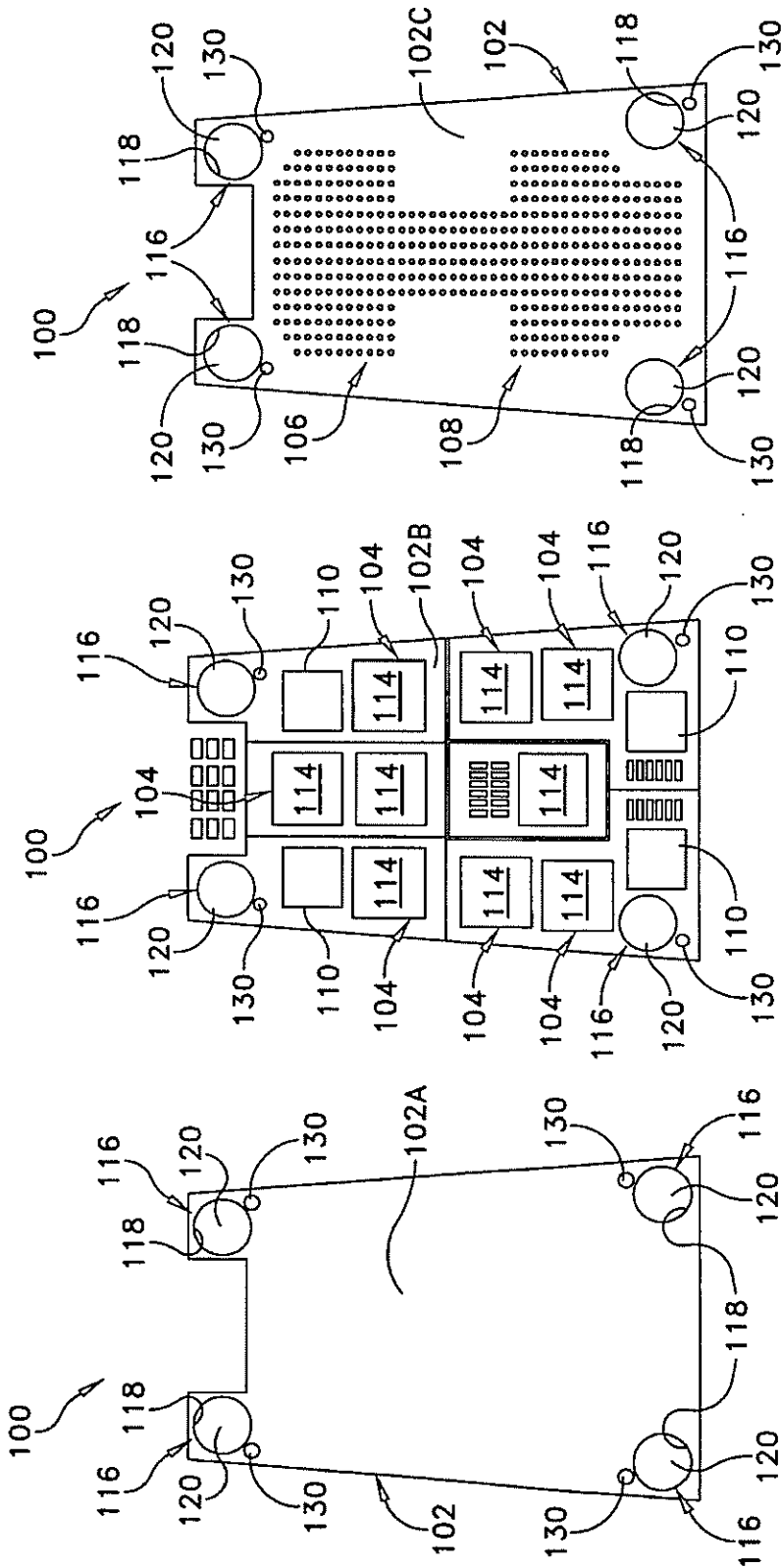


FIGURE 3

FIGURE 2

FIGURE 1

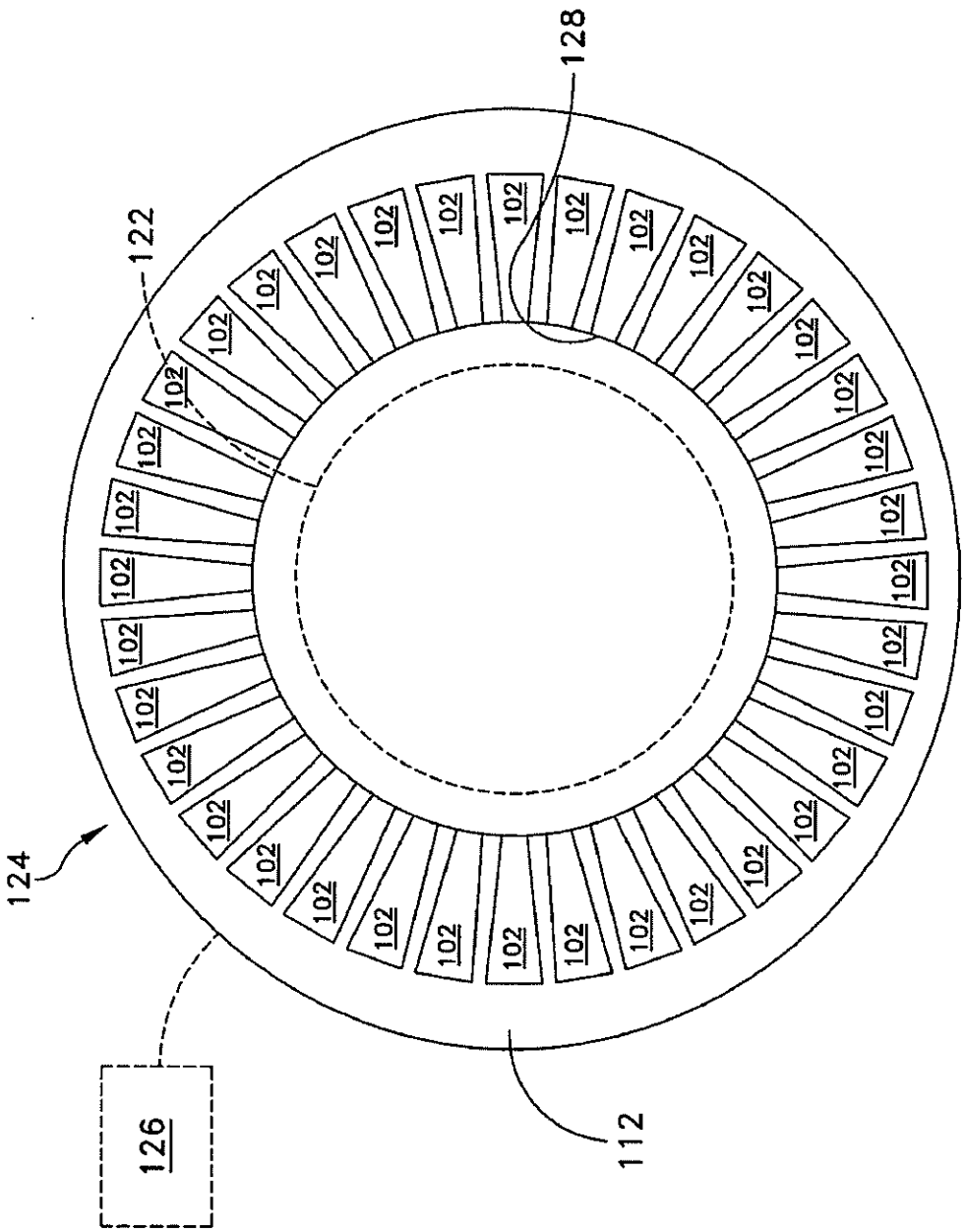


FIGURE 4

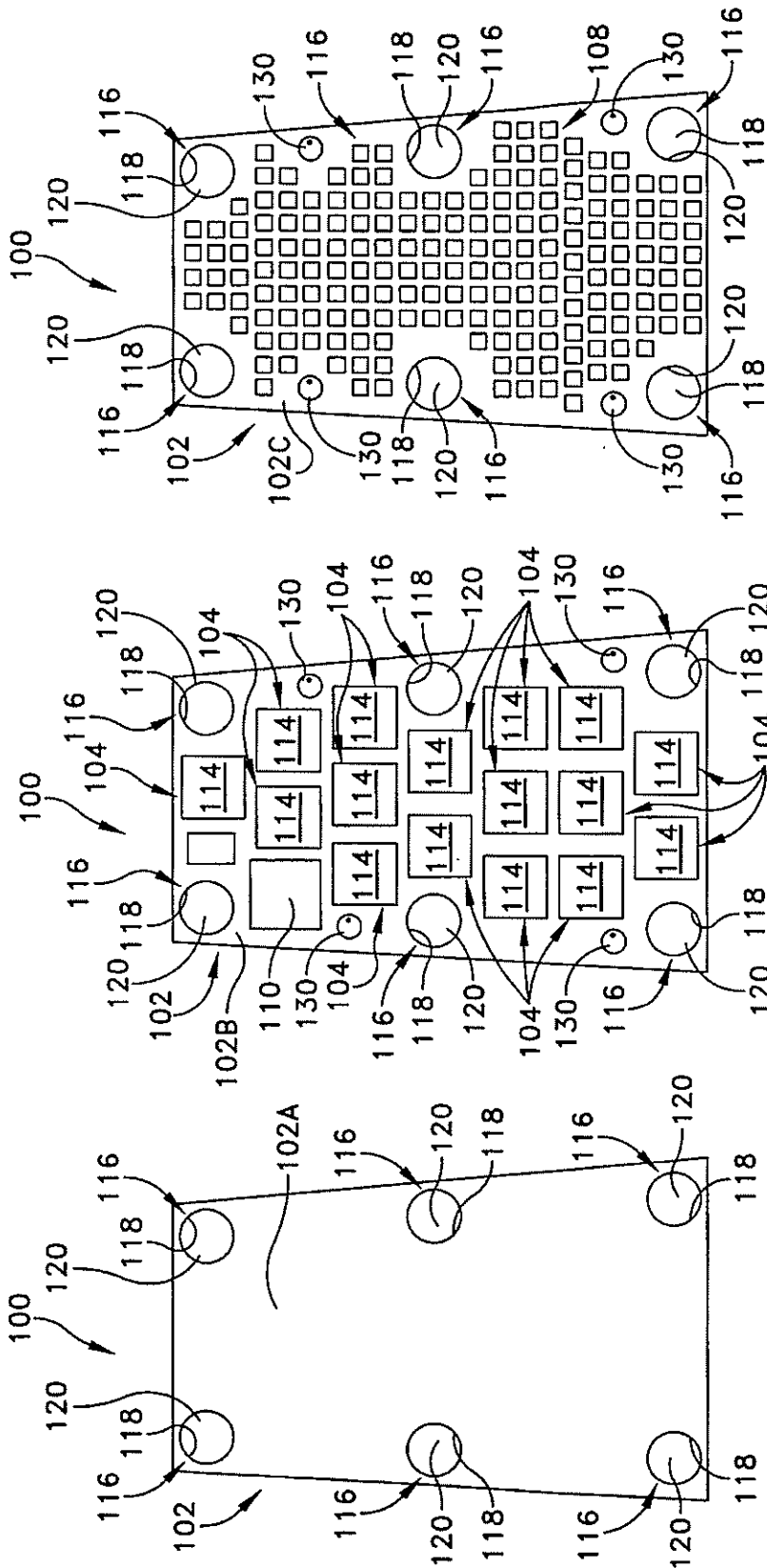


FIGURE 5

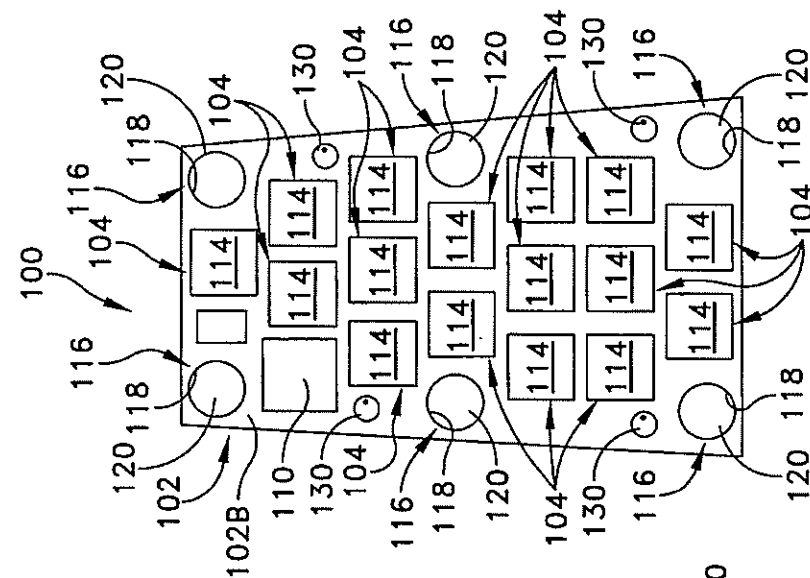


FIGURE 6

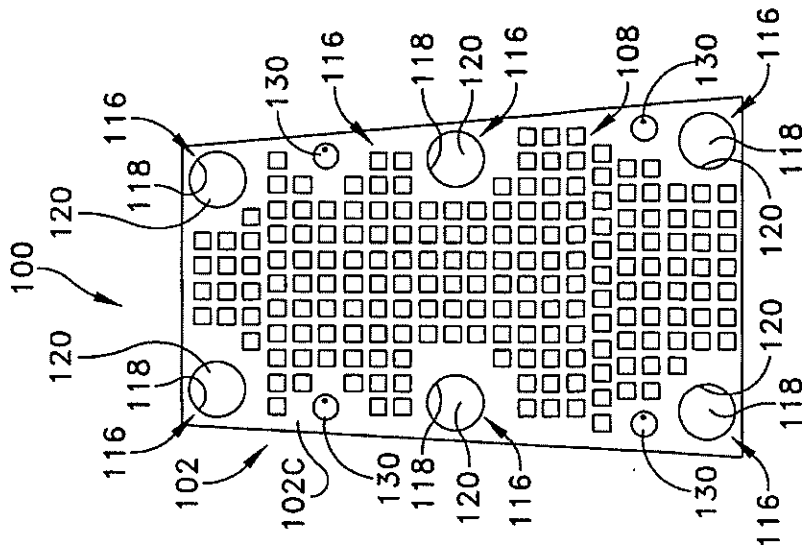


FIGURE 7

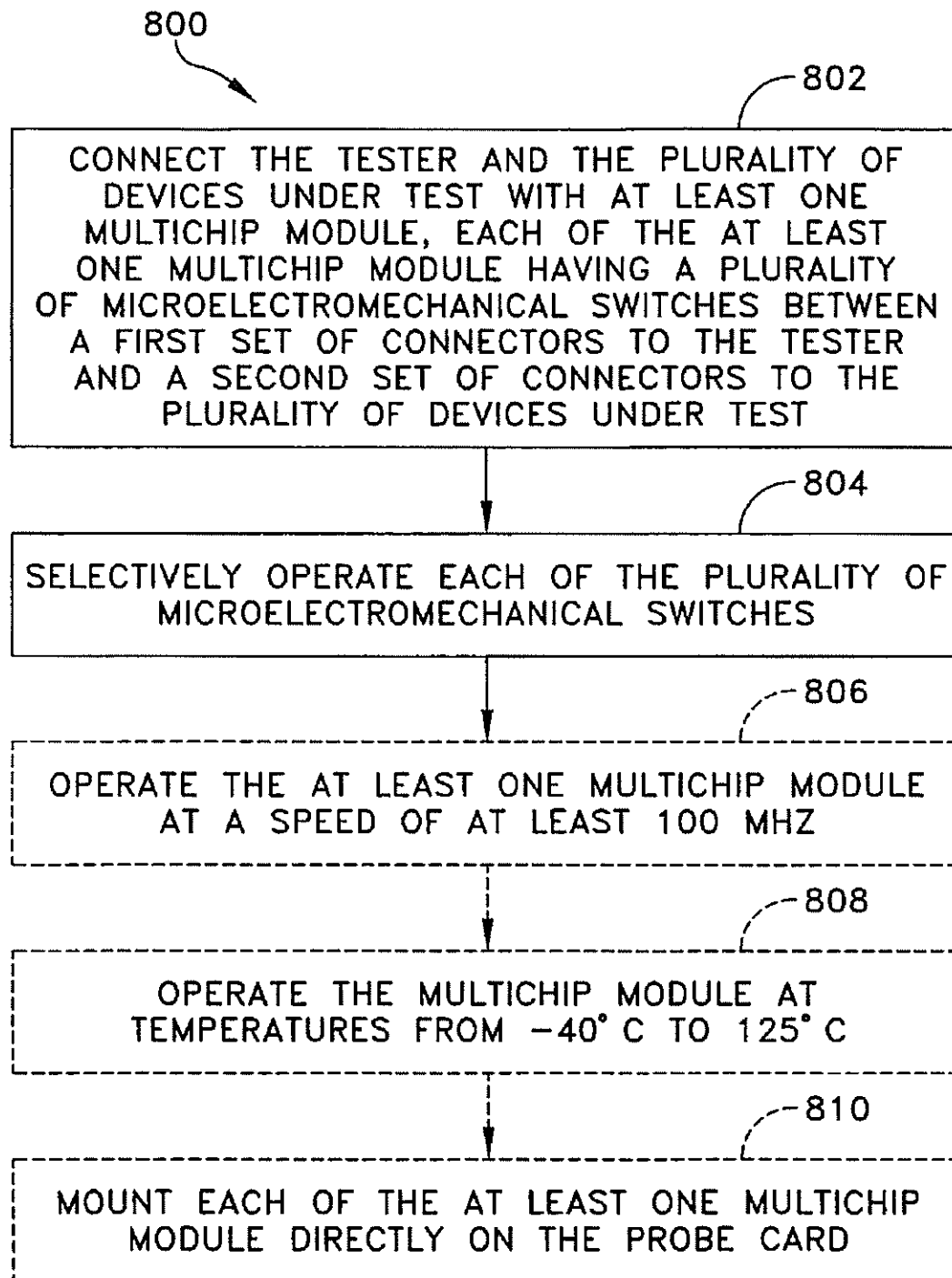


FIGURE 8

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**APPARATUS, SYSTEMS AND METHODS FOR
PROCESSING SIGNALS BETWEEN A TESTER
AND A PLURALITY OF DEVICES UNDER TEST
AT HIGH TEMPERATURES AND WITH SINGLE
TOUCHDOWN OF A PROBE ARRAY**

BACKGROUND

[0001] Others have developed solutions for two touch-down testing of 300 mm wafers containing many NAND dice, e.g. 432 NAND dice having 16 test sites each for a total of 6912 test sites. Generally, this type of testing utilizes mechanical relays installed in the device under test (DUT) interface of the automatic test equipment (ATE) system. These relays are typically located electrically far away from the device under test (DUT). This distance may create a large impedance mismatch when reading back from the device. In addition, the maximum data rate for testing the device may be limited to only 20 MHz.

[0002] Mechanical relays are also quite expensive. For example, the typical mechanical relays may each cost about \$8.00. This may limit the return on investment (ROI) for the customer. Mechanical relays are generally rated for about 1 to 10 million test cycles. This may create reliability issues for the customer over time. Furthermore, mechanical relays are only rated for operation up to 85° C. This allows testing of NAND devices using mechanical relays at or below 85° C.

[0003] Other solutions for multiplexing a large number of tester pin electronics (PE) by mounting a plurality of daughter boards on probe cards. This will only allow two touch-down testing of 300 mm wafers of NAND dice. This daughter card approach has limitations with respect to temperature and density. The connector limits the density of switches that can be placed on the daughter card and the active silicon switches have a temperature limitation of 85° C. when using standard grade integrated chips.

SUMMARY OF THE INVENTION

[0004] In an embodiment, there is provided apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising at least one multichip module, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and at least one driver to selectively operate each of the plurality of micro-electromechanical switches.

[0005] In another embodiment, there is provided a system for testing a plurality of devices under test, the system comprising a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test; a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

[0006] In yet another embodiment, there is provided apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising at least one multichip module mounted directly on a probe card and operable at a temperature of at least 125° C., and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test.

[0007] In still another embodiment, there is provided a method of processing signals between a tester and a plurality of devices under test, the method comprising connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and selectively operating each of the plurality of micro-electromechanical switches.

[0008] Other embodiments are also disclosed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Illustrative embodiments of the invention are illustrated in the drawings, in which:

[0010] FIGS. 1-3 illustrate one exemplary embodiment of a multichip module for processing signals between a tester and a plurality of devices under test;

[0011] FIG. 4 illustrates a system having a probe card with a plurality of multichip modules for processing signals between a tester and a plurality of devices under test;

[0012] FIGS. 5-7 illustrate another exemplary embodiment of a multichip module for processing signals between a tester and a plurality of devices under test; and

[0013] FIG. 8 is a flow chart diagram illustrative of methods of processing signals between a tester and a plurality of devices under test.

**DETAILED DESCRIPTION OF AN
EMBODIMENT**

[0014] Referring to FIGS. 1-7, there is shown apparatus 100 for processing signals between a tester and a plurality of devices under test. In one embodiment, apparatus 100 may include various types of multichip modules 102, which are also referred to as MCMs 102. FIGS. 1-3 illustrate one exemplary embodiment of multichip module 102. FIGS. 4-7 illustrate another exemplary embodiment of multichip module 102.

[0015] A top cover 102A of multichip module 102 is shown in FIGS. 1 and 5. A cross-sectional plan view 102B of multichip module 102 is shown in FIGS. 2 and 6. A bottom portion 102C is shown in FIGS. 3 and 6.

[0016] Referring to FIGS. 2 and 5, and each multichip module 102 may include a plurality of micro-electromechanical switches 104, which are also referred to as MEMs 104, between a first set of connectors 106 to the tester and a second set of connectors 108 to the plurality of devices under test. Each multichip module may include at least one driver 110 to selectively operate each of the plurality of micro-electromechanical switches 104.

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[0017] Looking at FIG. 4, and in an embodiment, apparatus 100 for processing signals may include a configuration in which each of multichip modules 102 are mounted directly on a probe card 112. Due to the proximity of multichip modules 102 to probe card 112 and the devices under test (not shown), one or more of multichip modules 102 may operate at a speed of at least 100 MHz. In another embodiment, one or more of multichip modules 102 may operate at a speed above 20 MHz to about 100 MHz.

[0018] In an embodiment, one or more of multichip modules 102 may operate at a temperature with a range from about -40° C. to about 125° C. In another embodiment, one or more of multichip modules 102 may operate within a temperature range from about 85° C. to about 125° C.

[0019] In one embodiment, one or more of multichip modules 102 may be rated for at least 1 billion test cycles. Multichip modules 102 may be rated for 10 billion or more test cycles. This is due, at least in part, to the micro-electromechanical switches 104 that may be used instead of other types of switches.

[0020] Referring to FIGS. 2 and 6, and in an embodiment, the plurality of micro-electromechanical switches 104 may be housed in separate MEMS dice 114. In one embodiment, each of the separate MEMS dice 114 may include eight single pole triple throw switches (FIG. 2). In another embodiment, each of the separate MEMS dice 114 may include eight single pole double throw switches (FIG. 6).

[0021] Looking at FIGS. 1-3 and 5-7, an attachment component 116 may be provided to secure one or more of multichip modules 102. In an embodiment, attachment component 116 mounts multichip module 102 to probe card 112 (FIG. 4). Attachment component 116 may include passageways 118 through multichip module 102 for a set of screws 120 to mount the multichip module to probe card 112 (FIG. 4).

[0022] As MEM MCM 102 may be attached to probe card 112 using screws 120 or other fasteners, a new tester does not need to be purchased from a supplier of the ATE system. A customer may simply design a probe card and attach these MEM MCMS to the probe card and install this new probe card assembly onto an existing ATE system.

[0023] Generally, MCM 102 may be very thin to allow probe card 112 together with MCMS 102 to fit into an auto loader of a prober. Many screws 120 or other fasteners may be used to attach MCM 102 to probe card 112 to prevent warping.

[0024] In an embodiment, one or more of drivers 110 may be designed to supply an electrostatic potential to selectively activate a MEMS gate associated with one or more of the plurality of micro-electromechanical switches 104. One or more of drivers 110 may be a vacuum-fluorescent display driver die 110. In one embodiment, four drivers 110 (FIG. 2) act as an algorithmic pattern generating system (APGS) and supply the electrostatic potential to four separate DUTs independently of one another. In another embodiment, one driver 110 (FIG. 6) acts as an algorithmic pattern generating system (APGS) and supplies electrostatic potential to DUTs.

[0025] In one embodiment, the second set of connectors of multichip modules 102 attach to a probe array 122. This probe array 122 may have at least 6000 probe tip needles so

as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of probe array 122. For example, each multichip module 102 may test 12 DUTs, there may be 36 multichip modules in attachment to probe card 112 for a total of 432 DUTs, and there may be 16 test sites on each one of the DUTs for a total of 6912 test sites, which in turn requires 6912 probe tip needles.

[0026] Referring to FIG. 4, and in an embodiment, there is shown a system 124 for testing a plurality of devices under test. System 124 may include a set of tester electronics 126 to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test. System 124 may include probe card 112 with at least one multichip module 102 mounted directly on probe card 112. Each of the at least one multichip module 102 may include a plurality of micro-electromechanical switches 104 between a first set of connectors to the set of tester electronics 126 and a second set of connectors to the plurality of devices under test. System may include one or more drivers 110 to selectively operate each of the plurality of micro-electromechanical switches 104. System 124 may further include probe array 122 to transmit signals between the multichip modules 102 of probe card 112 and the plurality of devices under test.

[0027] In one embodiment, probe card 112 may have 36 multichip modules 102 mounted thereon. Each of multichip modules 102 may have a plurality of MEMS dice 114 thereon. Furthermore, each one of the plurality of MEMS dice 114 may each contain a plurality of switches 104. In one embodiment, switches 104 may include single pole triple throw switches. In another embodiment, switches 104 may include single pole double throw switches.

[0028] Looking at FIG. 1, and in an embodiment, each of multichip modules 102 may have 9 MEMS dice 114 thereon. In one embodiment, each of the 9 MEMS dice 114 may have 8 MEMS switches 104. Looking at FIG. 4, and in another embodiment, each of multichip modules 102 may have 16 MEMS dice 114 thereon. In an embodiment, each of the 16 MEMS dice 114 may have 8 MEMS switches 104.

[0029] Referring to FIGS. 3 and 7, and in an embodiment, each one multichip module 104 may be housed in a standard package configuration having 780 pins which may be configured on bottom portion 102C. A portion of the 780 pins form first set of connectors 106, which may provide electrical connection to tester electronics. Another portion of the 780 pins form second set of connectors 108, which may provide electrical connection to devices under test.

[0030] Probe card 112 may have a maximum diameter of 440 millimeters. Probe card 112 may form an opening 128 for probe array 122. In an embodiment, opening 128 has a minimum diameter of 330 millimeters. Probe card 112 may contain at least 36 of multichip modules 102 mounted thereon.

[0031] In an embodiment, probe array 112 may have at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of probe array 112.

[0032] In an embodiment, system 124 enables one touchdown testing of 300 mm wafers containing NAND devices to be tested up to 100 MHz by mounting micro-electromechanical multichip modules 102 very close to the DUTs.

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This one touchdown testing cannot be achieved by using mechanical relays or active silicon devices mounted on daughter boards. Daughter boards mounted on the probe cannot achieve the required density of switches because of the space required for connectors. Mechanical relays, which are mounted far from the DUTs, are generally limited to about 20 MHz and cannot achieve a data rate near 100 MHz.

[0033] For example, and looking at FIGS. 1-3, to achieve a desired data rate of about 20 MHz to about 100 MHz, 72 single-pole, triple-throw (SPTT) MEM switches 104 and four vacuum-florescent display driver dice (VFD) 110 may be integrated into one 780 pin multichip module (MCM) 102. This MCM 102 may measure 26 mm×55 mm×34 mm×55 mm (see FIG. 1).

[0034] In one embodiment, and looking at FIGS. 5-7, to achieve a desired data rate of about 20 MHz to about 100 MHz, 128 single-pole, double-throw (SPDT) MEM switches 104 and one vacuum-florescent display driver die (VFD) 110 with 32 outputs may be integrated into one 780 pin multichip module (MCM) 102. This MCM 102 may measure 26 mm×55 mm×34 mm×55 mm (see FIG. 5).

[0035] MEM MCMs 102 may be fabricated quite inexpensively. For example, an MCM package containing 128 SPDT switches with only 780 pins may cost about \$300 per package. This drastically improves the return on investment (ROI) for the customer.

[0036] As discussed above, mechanical relays are generally rated a maximum testing temperature of 85° C., which is due to the moving parts inside the relay housing. Implementations using active silicon devices are also typically rated for a maximum testing temperature of 85° C. Using either of these, i.e. mechanical relays or daughter boards with active silicon, NAND devices may only be tested up to 85° C. However, using system 100, NAND devices may be tested at temperatures ranging from -40° C. to 125° C. with one or more of MEM MCMs 102.

[0037] MEM MCMs 102 are generally mounted very close to the DUTs so as to increase the maximum data rate for testing NAND devices from 20 MHz to 100 MHz, and also to enable testing of the entire 300 mm wafer with one touchdown.

[0038] Utilizing MEM MCMs 102 instead of mechanical relays is also more cost effective and more reliable. A typical mechanical relay is rated for 1-10 million cycles. A typical MEM MCM 102 may be rated for 1-10 billion cycles. Using daughter boards limits the density of switches that can be mounted on the probe card due to the space required for connectors.

[0039] Multichip modules 102 are generally capable of much higher densities than daughter cards. Mounting multichip modules 102 onto probe card 112 enables the customer to double the pin count of the test system when testing NAND devices without buying a new ATE system.

[0040] Using the Agilent V5400 test system, 16 NAND devices with 36 test sites each may be tested. Each MEMs dice may have 8 SPDT switches. The electrostatic potential required to activate the MEMs gate will be supplied by a vacuum-florescent display driver die 110 located inside the MCM package 102. MCM substrate 102B may be a blind and buried via substrate made of NELCO 4000-13 Si, which

is a typical MCM substrate. Connectors 106 and connectors 108 may include, but are not limited to pins. Such pins of the package may include Be—Cu springs that are attached with silver epoxy to the bottom of the NELCO 4000-13 Si substrate. MEMs 104 and single VFD 110 may be located inside MCM 102 and may be wired bond or soldered to the substrate.

[0041] In an embodiment, MCMs 102 may be reusable. MCMs 102 can be transferred from one probe card to another when the probe card becomes damaged or is simply obsolete due to a change in die size or layout on the wafers.

[0042] Alignment pins 130 may be provided to align MCM 102 to probe card 112.

[0043] Looking now at FIG. 8, and in an embodiment, there is provided a method 800 of processing signals between a tester and a plurality of devices under test. Method 800 may include connecting 802 the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test. Method 800 may include selectively operating 804 each of the plurality of micro-electromechanical switches.

[0044] In one embodiment, method 800 may further include operating 806 the at least one multichip module at a speed of at least 100 MHz. In an embodiment, method 800 may include operating 808 the multichip module at temperatures from -40° C. to 125° C.

[0045] Method 800 may include mounting 810 each of the at least one multichip module directly on the probe card.

1. Apparatus for processing signals between a tester and a plurality of devices under test, the apparatus comprising:

at least one multichip module, each of the at least one multichip module comprising:

a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

at least one driver to selectively operate each of the plurality of micro-electromechanical switches.

2. Apparatus in accordance with claim 1, further comprising a probe card on which each one of the at least one multichip module is directly mounted.

3. Apparatus in accordance with claim 1, further comprising a plurality of MEMs dice on which the plurality of micro-electromechanical switches are formed.

4. Apparatus in accordance with claim 1, wherein the separate MEMs dice each include eight single pole triple throw switches.

5. Apparatus in accordance with claim 1, further comprising an attachment component for each one of the at least one multichip module, and wherein the attachment component mounts the multichip module to a probe card.

6. Apparatus in accordance with claim 5, wherein the attachment component includes passageways through the multichip module for a set of screws to mount the multichip module to the probe card.

7. Apparatus in accordance with claim 1, wherein the driver is designed to supply an electrostatic potential to

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activate a MEMS gate associated with each of the plurality of micro-electromechanical switches.

8. Apparatus in accordance with claim 1, wherein the at least one driver comprises a vacuum-florescent display driver dice.

9. A system for processing signals between a tester and a plurality of devices under test, the system comprising:

at least one multichip module mounted directly on a probe card and operable at a temperature of at least 125° C., and each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test.

10. A system in accordance with claim 9, wherein the second set of connectors attach to a probe array having at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

11. A system for testing a plurality of devices under test, the system comprising:

a set of tester electronics to generate signals for application to the plurality of devices under test, and to receive signals generated by the plurality of devices under test;

a probe card with at least one multichip module mounted thereon, each of the at least one multichip module comprising a plurality of micro-electromechanical switches between a first set of connectors to the set of tester electronics and a second set of connectors to the plurality of devices under test, and a driver to selectively operate each of the plurality of micro-electromechanical switches; and

a probe array to transmit signals between the at least one multichip module of the probe card and the plurality of devices under test.

12. A system in accordance with claim 11, wherein each of the at least one multichip modules has a plurality of MEMS dice thereon.

13. A system in accordance with claim 11, wherein each one of the plurality of MEMS dice each contain a plurality of micro-electromechanical switches.

14. A system in accordance with claim 13, wherein the switches are single pole triple throw switches.

15. A system in accordance with claim 13, wherein the switches are single pole double throw switches.

16. A system in accordance with claim 11, wherein the probe card has a maximum diameter of 440 millimeters.

17. A system in accordance with claim 16, wherein the probe card forms an opening for the probe array, and the opening has a minimum diameter of 330 millimeters.

18. A system in accordance with claim 11, wherein the probe array has at least 6000 probe tip needles so as to test at least 6000 test sites of the plurality of devices under test during a single touchdown of the probe array.

19. A method of processing signals between a tester and a plurality of devices under test, the method comprising:

connecting the tester and the plurality of devices under test with at least one multichip module, each of the at least one multichip module having a plurality of micro-electromechanical switches between a first set of connectors to the tester and a second set of connectors to the plurality of devices under test; and

selectively operating each of the plurality of micro-electromechanical switches to process the signals between individual ones of the first set of connectors to the tester and selected multiple ones of the second set of connectors to the plurality of devices under test.

20. A method in accordance with claim 19, further comprising operating the at least one multichip module at a speed of at least 100 MHz.

21. A method in accordance with claim 19, further comprising operating the multichip module at a temperature of at least 125° C.

22. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card.

23. A method in accordance with claim 19, further comprising mounting each of the at least one multichip module directly on the probe card, operating the multichip module at a temperature of at least 125° C., and operating the at least one multichip module at a speed of at least 100 MHz.

* * * * *